

MULTI-CHIP STACK FLIP-CHIP PACKAGE

FIELD OF THE INVENTION

The present invention is generally relating to a multi-chip package (MCP), particularly to a multi-chip stack flip-chip package.

BACKGROUND OF THE INVENTION

It is well known that a multi-chip flip-chip package includes a plurality of flip chips with the bumps and a substrate for directly flip-chip mounting. In US patent No.6,507,098, Lo et al. disclosed a structure of a multi-chip stack package, which comprises a plurality of flip chips mounted on one surface of substrate. Each flip chip has a plurality of bumps on an active surface thereof for flip-chip (C4) mounting on the same surface of the substrate. The substrate is demanded to supply a large enough area for mounting the flip chips. However, the multi-chip flip-chip package can't achieve a vertical stack with the plurality of the flip chips. In addition, the substrate is a well-known printed circuit board (PCB), the minimum pitch of bump pads of the PCB substrate is about 200 μm (micrometer) according to current PCB technology, it is difficult to manufacture the substrate with pitch of bump pads less than 150 μm by means of PCB process. However the wiring pitch of the integrated circuits of the flip chip has reached 0.1 μm up-to-now which means that the chip size becomes smaller and smaller, and the bumps on the flip chip are more crowded. Normally the pitch of bumps of the flip chip is around 150 μm , even near to 70~90 μm for special design, so the pitch of bumps of the flip chip and the pitch of bump pads of the PCB become unmatchable. Therefore, the yield of mass production of multi-chip flip-chip package cannot reach the acceptable range because it is not easy to make a substrate with bump pads in tiny pitch.

In US patent No.5,923,090, Fallon et al. also disclosed another well-known stacked multi-chip package. The package comprises an integrated circuit chip by wire bonding and a flip chip. The integrated circuit chip is attached to a substrate, and the flip chip is mounted on a major surface of the integrated circuit chip. The integrated circuit chip

1 has an extra circuitry (C4 connection pad) on the major surface different from a normal
2 chip in order to bond the flip chip. Pads on periphery of the major surface of the
3 integrated circuit chip are connected with the substrate by bonding wires. It is necessary
4 that size of the integrated circuit chip is larger than that of the flip chip. But it is very
5 hard to design the C4 connection pads, bond pads and extra circuitry on the major surface
6 of the integrated circuit chip.

7 SUMMARY

8 It is a first object of the present invention to provide a multi-chip stack flip-chip
9 package including a dummy chip attached to a first flip chip on a substrate. The dummy
10 chip has a redistribution layer (RDL) without active electrical function. A second flip
11 chip is mounted on the dummy chip. The redistribution layer of the dummy chip
12 electrically connects the second flip chip with the substrate skipping over the first flip
13 chip to assemble a multi-chip package enabling the plurality of flip chips to be stacked
14 repeatedly.

15 It is a second object of the present invention to provide a multi-chip stack flip-chip
16 package including a dummy chip. The dummy chip has a redistribution layer (RDL)
17 without active electrical function and a flip chip is mounted on the dummy chip. The
18 dummy chip with the redistribution layer is an electrically connecting interface to connect
19 the flip chip to a PCB substrate, and the dummy chip is attached to back surface of
20 another flip chip or PCB substrate for flip chip stacking.

21 In accordance with the present invention, a multi-chip stack flip-chip package
22 comprises a substrate having a top surface and a bottom surface, such as printed circuit
23 board (PCB). At least a first flip chip is disposed on the top surface of the substrate. A
24 dummy chip is attached to back surface of the first flip chip and has a redistribution layer
25 for electrically connecting to at least a second flip chip. The redistribution layer on a
26 surface of the dummy chip includes a plurality of bump pads, a plurality of peripheral
27 pads and a plurality of integrated circuit traces connecting the bump pads and the

1 peripheral pads. The peripheral pads are arranged on periphery of upper surface of the
2 dummy chip. The second flip chip is mounted on the dummy chip and connected with
3 the bump pads of the redistribution layer by bumps. Further the peripheral pads of the
4 redistribution layer are electrically connected with the substrate by electrically connecting
5 devices, such as bonding wires or TAB leads, in order to vertically stack the plurality of
6 flip chips.

7 DESCRIPTION OF THE DRAWINGS

8 Fig.1 is a cross-sectional view of the first embodiment of a multi-chip stack flip-chip
9 package in accordance with the present invention.

10 Fig.2 is a top view of the first embodiment of the multi-chip stack flip-chip package
11 in accordance with the present invention.

12 Fig.3 is a cross-sectional view of the second embodiment of the multi-chip stack
13 flip-chip package in accordance with the present invention.

14 DETAILED DESCRIPTION OF THE PRESENT INVENTION

15 Referring to Fig.1, a multi-chip stack flip-chip package 100 in accordance with the
16 first embodiment of the present invention comprises a substrate 110, at least a first flip
17 chip 120, a dummy chip 130 and at least a second flip chip 140. The substrate 100 is a
18 printed circuit board (PCB) formed by metal foil and glass fiber reinforced resin
19 including BT resin, FR-4 resin or FR-5 resin. The substrate 100 has a top surface 111
20 and a bottom surface 112.

21 The first flip chip 120 is a chip with active electrical function, such as micro
22 processor, micro controller, memory or Application Specific Integrated Circuit (ASIC).
23 The first flip chip 120 has an active surface and a corresponding back surface. The first
24 flip chip 120 includes a plurality of bumps 121 on its active surface. The first flip chip
25 120 is disposed on the top surface 111 of the substrate 110 by flip-chip mounting.
26 Alternatively, the first flip chip 120 can be mounted on another dummy chip or a
27 wire-bonding chip on the substrate 110 (not shown in the figure).

1 Normally the second flip chip 140 has a plurality of bumps 141 on its active surface
2 and can be mounted on the dummy chip 130 to be a chip assembly in advance. The
3 dummy chip 130 is attached to back surface of the first flip chip 120 by an adhesive layer
4 122. Preferably, the dummy chip 130 is larger than the first flip chip 120 in size. The
5 dummy chip 130 is a silicon substrate without active electrical function but has a
6 redistribution layer 131 (RDL) formed by integrated circuit manufacturing process.
7 Referring to Fig.1 and 2, the redistribution layer 131 includes a plurality of bump pads
8 132, a plurality of peripheral pads 133 and a plurality of integrated circuit traces 134
9 connecting the bump pads 132 and the peripheral pads 133. The peripheral pads 133 are
10 arranged on periphery of upper surface of the dummy chip 130, and the bump pads 132
11 are corresponding to the bumps 141 of the second flip chip 140 in array or the other.
12 Preferably the bump pads 132 have a pitch smaller than that of the peripheral pads 133 to
13 fully match pitch of the bumps 141 of the second flip chip 140. The bump pads 132, the
14 peripheral pads 133 and the integrated circuit traces 134 of the redistribution layer 131
15 are formed on upper surface of the dummy chip 130 by integrated circuit manufacturing
16 process. For example, a metal layer is sputtered on the upper surface of the dummy chip
17 130. After forming a photoresist, exposing the photoresist and etching the metal layer,
18 then the redistribution layer 131 is formed. Preferably, a passivation layer is coated on
19 the redistribution layer 131 to cover the integrated circuit traces 134 (not shown in the
20 figure). The bumps 141 of the second flip chip 140 are bonded on the bump pads 132 of
21 the redistribution layer 131.

22 After attaching the dummy chip 130 on the first flip chip 120, the peripheral pads
23 133 are electrically connected to the substrate 110 by a plurality of electrically
24 connecting devices 135, such as bonding wires or TAB leads. The redistribution layer
25 131 of the dummy chip 130 enables the pitch of the bump pads 132 ($< 150\ \mu\text{m}$) to be
26 much smaller than that of connecting point of substrate 110. In addition, an insulation
27 compound 150 is formed on the top surface 111 of the surface 110 to protect the first flip

1 chip 120, the second flip chip 140, the dummy chip 130 and the electrical connecting
2 devices 135 by molding. The solder balls 160 are bonded on the bottom surface 112 of
3 the substrate 110 for being outer terminals of the package 100. The dummy chip 130 is
4 an electrically connecting interface for connecting the second flip chip 140 stacked on the
5 flip chip 120 with the substrate 110. Thus the multi-chip flip-chip package 100 can
6 repeatedly stack the plurality of flip chips 120,140 without increasing the size of the
7 substrate 110. Moreover, the bump pads 132 of the dummy chip 130 can fully match
8 bumps 141 of the second flip chip 140 in fine pitch to achieve a complete flip chip
9 stacking under same advanced IC technology. The dummy chip 130 is larger than the
10 second flip chip 140 in size so that the electrically connecting devices 135 may connect
11 the peripheral pads 133 of the dummy chip 130 to the substrate 110. In this present
12 invention, the size of the second flip chip 140 is not limited, may be larger, smaller or
13 equal to the first flip chip 120. Furthermore, another dummy chip mounting with flip
14 chip(s) (not shown in the drawing) is able to stack on the second flip chip 140 and is
15 sealed inside the single insulation compound 150 to assemble a multi-chip stack flip-chip
16 package, so the multi-chip stack flip-chip package 100 of the present invention is suitable
17 for the plurality of flip chips in vertical stack configuration.

18 Referring to Fig.3, a multi-chip stack flip-chip package 200 in accordance with the
19 second embodiment of the present invention comprises a substrate 210, at least a flip chip
20 220 and a dummy chip 230. The substrate 210 is a printed circuit board, such as BGA
21 substrate, motherboard or memory module substrate. The substrate 210 has a top
22 surface 211. The dummy chip 230 has a redistribution layer 231 formed by integrated
23 circuit manufacturing process, and the redistribution layer 231 includes a plurality of
24 bump pads 232, a plurality of peripheral pads 233 and a plurality of integrated circuit
25 traces connecting the bump pads 232 with the peripheral pads 233. The peripheral pads
26 233 are arranged on the periphery of upper surface of the dummy chip 230 for electrically
27 connecting to the substrate 210. The flip chip 220 is mounted on upper surface of the

1 dummy chip 230 so that the bumps 221 of the flip chip 220 are bonded onto the bump
2 pads 232 of the redistribution layer 213. Preferably the flip chip 220 is mounted on the
3 dummy chip 230 in wafer form to manufacture a chip assembly in advance. The
4 dummy chip 230 is attached to the top surface 211 by epoxy adhesive or PI adhesive film.
5 The dummy chip 230 is configured to be an electrically connecting interface between the
6 flip chip 220 and the substrate 210 to achieve fine pitch flip-chip mounting. Electrically
7 connecting devices 234 connect the peripheral pads 233 of the dummy chip 230 to the
8 substrate 210 so as to electrically connect the flip chip 220 with the substrate 210 through
9 the dummy chip 230. An insulation compound 240 is formed on the substrate 210 by
10 coating or dispensing to protect the flip chip 220 and the electrically connecting devices
11 234.

12 Although the preferred embodiments of the invention have been disclosed for
13 illustrative purposes, those skilled in the art will appreciate that various modifications,
14 additions and substitutions are possible, without departing from the scope and spirit of the
15 invention as disclosed in the accompanying claims.

16
17
18
19
20
21
22
23
24
25
26
27